Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) A method of manufacturing an electronic device comprising thin-film circuit elements that include a diode integrated with a crystalline thin-film transistor, the transistor having a channel area in an active semiconductor film that is more crystalline than an active semiconductor film of the diode, comprising:

~~a film formation step including~~ forming on a circuit substrate the crystalline active semiconductor film of the transistor with a first process involving a first processing temperature;

~~a regions forming step including~~ forming doped source and drain regions of the transistor at ends of the channel area with a second process involving a second processing temperature;

~~a film provisioning step including~~ providing an interconnection film between an electrode area of the transistor and a diode area over which the diode is to be formed, and providing an etch-stop film on which the active semiconductor film for the diode is to be deposited;

~~a film depositing step thereafter including~~ depositing the active semiconductor film for the diode over the interconnection film and the etch-stop film with a third process that involves a third processing temperature, ~~the film depositing step being performed after the film formation step and the regions forming step, and~~ the first and second processing temperatures being higher than the third processing temperature; and

~~an etching step thereafter including~~ etching away the active semiconductor film for the diode from over the etch-stop film to leave the active semiconductor film for the diode over the interconnection film in the diode area.

2. (Previously presented) The method of claim 1, wherein the etch-stop film is an insulating film that extends over the interconnection film and that has a window at the diode

area to permit contact between the interconnection film and the active semiconductor film of the diode.

3. (currently amended) The method of claim 2, wherein the diode has its active semiconductor film forming an intrinsic region between P and N electrode regions of a vertical PIN diode structure, and wherein the interconnection film comprises a doped region ~~that is formed in the regions forming step~~ in a semiconductor film together with the doped source and drain regions of the transistor and a bottom one of the P and N electrode regions of the PIN diode.

4. (currently amended) The method of claim 3, wherein regions of the crystalline active semiconductor film ~~provided in the film formation step~~ are doped ~~in the regions forming step~~ to provide the source and drain regions of the transistor, the bottom one of the P and N electrode regions of the PIN diode, and the interconnection film therebetween.

5. (currently amended) The method of claim 3, wherein at least a portion of the interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a doped-semiconductor top gate electrode of the transistor which is ~~thereby~~ interconnected with the bottom one of the P and N electrode regions of the PIN diode.

6. (Previously presented) The method of claim 5, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

7. (currently amended) The method of claim 4, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by ~~means of~~ the ~~same~~ interconnection film, and wherein the interconnection film provides the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and/or the source and drain regions of the second transistor.

8. (currently amended) The method of claim 1, wherein the interconnection film comprises metal which ~~itself~~ provides the etch-stop film, and the diode has a vertical PIN diode structure formed in its active semiconductor film as an intrinsic region between P and N electrode regions.

9. (currently amended) The method of claim 8, wherein at least a portion of the etch-stop interconnection film is provided on a gate-dielectric film on the crystalline active semiconductor film to form a top gate electrode of the transistor which is ~~thereby~~ interconnected with a bottom one of the P and N electrode regions of the PIN diode.

10. (Previously presented) The method of claim 9, wherein the PIN diode is formed on the gate-dielectric film on the crystalline active semiconductor film of the transistor.

11. (currently amended) The method of claim 9, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by ~~means of~~ the ~~same~~ interconnection film, and wherein the interconnection film connects the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and the source region of the second transistor.

12. (Previously presented) The method of claim 7, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode in each pixel, and wherein the light-emitting diode is driven via the first transistor as addressed via the second transistor.

13. (currently amended) The method of claim 1, wherein the crystalline semiconductor film is subjected to a hydrogenation process ~~that is performed after the film formation step and the regions forming step and before stage film depositing step~~.

14. (currently amended) The method of claim 1, wherein the crystalline semiconductor film is formed ~~in the film formation step~~ by crystallising a deposited semiconductor film using laser heating of the film.

15. (currently amended) The method of claim 1, wherein the doped source and drain regions are formed ~~in the regions forming step~~ by an ion implant of dopant in the crystalline semiconductor film and by annealing the implanted dopant.

16-18 (Canceled)

19. (currently amended) The method of claim 5, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by ~~means of~~ the ~~same~~ interconnection film, and wherein the interconnection film provides the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and/or the source and drain regions of the second transistor.

20. (currently amended) The method of claim 10, wherein the electronic device comprises first and second crystalline thin-film transistors integrated with the PIN diode by ~~means of~~ the ~~same~~ interconnection film, and wherein the interconnection film connects the bottom one of the P and N electrode regions of the PIN diode, the top gate electrode of the first transistor, and the source region of the second transistor.

21. (Previously presented) The method of claim 11, wherein the electronic device comprises an active-matrix electroluminescent display with a light-emitting diode in each pixel, and wherein the light-emitting diode is driven via the first transistor as addressed via the second transistor.